CLAIMS

What is claimed is:

1. A bandgap reference circuit comprising:

an operational amplifier including a first input, a second input, and a first output;

a T-network of passive resistors electrically connected between said first and said second inputs, wherein said T-network includes:

a first resistor having a first terminal and a second terminal, wherein said first terminal is electrically connected to said first input,

a second resistor having a third terminal and a fourth terminal, wherein said third terminal is electrically connected to said second terminal and said fourth terminal is electrically connected to said second input, and

a third resistor having a fifth terminal and a sixth terminal, wherein said fifth terminal is electrically connected to at least one of said second and said third terminals and said sixth terminal is electrically connected to a reference potential; and

a transistor network having a third input and a second output, wherein said first output of said operational amplifier is electrically connected to said third input to generate a bandgap reference voltage at said second output.

2. The bandgap reference circuit of claim 1, wherein said transistor network is a CMOS transistor network.

3. The bandgap reference circuit of claim 2, wherein said CMOS transistor network includes:

a first CMOS transistor having a gate electrically connected to said first output, a source electrically connected to a supply voltage, and a drain electrically connected to a diode, wherein said drain of said first CMOS transistor is configured to function as said first input;

a second CMOS transistor having a gate electrically connected to said first output, a source electrically connected to said supply voltage, and a drain electrically

connected to a diode-resistor network, wherein said drain of said second CMOS transistor is configured to function as said second input; and

a third CMOS transistor having a gate electrically connected to said first output, a source electrically connected to said supply voltage, and a drain electrically connected to a fourth resistor, wherein said drain of said third CMOS transistor is configured to function as said second output.

4. The bandgap reference circuit of claim 3, wherein each of said first, second, and third CMOS transistors is a P-substrate MOS.

5. The bandgap reference circuit of claim 3, wherein an anode of said diode is electrically connected to said drain of said first CMOS transistor and a cathode of said diode is electrically connected to said reference potential.

6. The bandgap reference circuit of claim 3, wherein said fourth resistor includes a seventh terminal and an eighth terminal, wherein said seventh terminal is electrically connected to said drain of said third CMOS transistor and said eighth terminal is electrically connected to said reference potential.

7. The bandgap reference circuit of claim 3, wherein said diode-resistor network includes:

a fifth resistor having a seventh terminal and an eighth terminal, wherein said seventh terminal is electrically connected to said drain of said second CMOS transistor; and

one or more diodes electrically connected in parallel, wherein anodes of said one or more diodes are electrically connected to said eighth terminal and cathodes of said one or more diodes are electrically connected to said reference potential.

8. The bandgap reference circuit of claim 7, wherein said first resistor has a value of 100kΩ, said second resistor has a value of 100kΩ, said third resistor has a value of 1.6MΩ, said fourth resistor has a value of 800kΩ, and said fifth resistor has a value of 220kΩ.

9. The bandgap reference circuit of claim 2, wherein said CMOS transistor network includes:

a first CMOS transistor having a gate connected to said first output and a source electrically connected to a supply voltage, wherein a drain of said first CMOS transistor is configured to function as said first input;

a diode having an anode and a cathode, wherein the drain of said first CMOS transistor is electrically connected to said anode and said reference potential is electrically connected to said cathode;

a second CMOS transistor having a gate electrically connected to said first output and a source electrically connected to said supply voltage, wherein a drain of said second CMOS transistor is configured to function as said second input;

a diode-resistor network including:

a fourth resistor having a seventh terminal and an eighth terminal, wherein said seventh terminal is electrically connected to the drain of said second CMOS transistor, and

a plurality of diodes electrically connected in parallel, wherein anodes of said plurality of diodes are electrically connected to said eighth terminal and cathodes of said plurality of diodes are electrically connected to said reference potential;

a third CMOS transistor having a gate electrically connected to said first output and a source electrically connected to said supply voltage, wherein a drain of said third CMOS transistor is configured to function as said second output; and

a fifth resistor having a ninth terminal and a tenth terminal, wherein said ninth terminal is electrically connected to the drain of said third CMOS transistor and said tenth terminal is electrically connected to said reference potential.

10. The bandgap reference circuit of claim 1, wherein said first input is an inverting input of said operational amplifier and said second input is a non-inverting input of said operational amplifier.

11. In a bandgap reference circuit having:

an operational amplifier including a first input, a second input, and an output;

a first CMOS transistor having a gate connected to said first output, a source connected to a supply voltage, and a drain connected to a diode, wherein said drain of said first CMOS transistor is configured to function as said first input;

a second CMOS transistor having a gate connected to said first output, a source connected to said supply voltage, and a drain connected to a first resistor in series with a parallel network of diodes, wherein said drain of said second CMOS transistor is configured to function as said second input;

a third CMOS transistor having a gate connected to said output, a source connected to said supply voltage, and a drain connected to a second resistor, wherein a bandgap reference voltage is obtained at said drain of said third CMOS transistor;

the improvement comprises:

a T-network of passive resistors connected between said first and said second inputs, wherein said T-network includes:

a third resistor having a first terminal and a second terminal, wherein said first terminal is electrically connected to said first input,

a fourth resistor having a third terminal and a fourth terminal, wherein said third terminal is electrically connected to said second terminal and said fourth terminal is electrically connected to said second input, and

a fifth resistor having a fifth terminal and a sixth terminal, wherein said fifth terminal is electrically connected to at least one of said second and said third terminals and said sixth terminal is electrically connected to a reference potential.

12. The improvement of claim 11, wherein said third resistor has a value of 100kΩ, said fourth resistor has a value of 100kΩ, and said fifth resistor has a value of 1.6MΩ.

13. The improvement of claim 11, wherein said first input is an inverting input of said operational amplifier and said second input is a non-inverting input of said operational amplifier.

14. A method comprising:

providing an operational amplifier having a first input, a second input, and a first output;

connecting a T-network of passive resistors between said first and said second inputs, wherein said T-network includes:

a first resistor having a first terminal and a second terminal, wherein said first terminal is connected to said first input,

a second resistor having a third terminal and a fourth terminal, wherein said third terminal is connected to said second terminal and said fourth terminal is connected to said second input, and

a third resistor having a fifth terminal and a sixth terminal, wherein said fifth terminal is connected to at least one of said second and said third terminals and said sixth terminal is connected to a reference potential; and

further providing a transistor network having a third input and a second output, wherein said first output of said operational amplifier is connected to said third input.

15. The method of claim 14, wherein further providing said transistor network includes:

providing a first CMOS transistor having a gate connected to said first output, a source connected to a supply voltage, and a drain connected to a diode, wherein said drain of said first CMOS transistor is configured to function as said first input;

providing a second CMOS transistor having a gate connected to said first output, a source connected to said supply voltage, and a drain connected to a diode-resistor network, wherein said drain of said second CMOS transistor is configured to function as said second input; and

providing a third CMOS transistor having a gate connected to said first output, a source connected to said supply voltage, and a drain connected to a fourth resistor, wherein said drain of said third CMOS transistor is configured to function as said second output.

16. A method of generating a bandgap reference voltage, said method comprises:

using an operational amplifier having a first input, a second input, and a first output;

using a T-network of passive resistors between said first and said second inputs, wherein

said T-network includes:

a first resistor having a first terminal and a second terminal, wherein said first terminal is connected to said first input;

a second resistor having a third terminal and a fourth terminal, wherein said third terminal is connected to said second terminal and said fourth terminal is connected to said second input; and

a third resistor having a fifth terminal and a sixth terminal, wherein said fifth terminal is connected to at least one of said second and said third terminals and said sixth terminal is connected to a reference potential;

further using a transistor network having a third input and a second output, wherein said first output of said operational amplifier is connected to said third input; and

biasing said operational amplifier and said transistor network so as to generate said bandgap reference voltage at said second output.